



# ಬಿ.ಎಂ.ಎಸ್. ತಾಂತ್ರಿಕ ಮತ್ತು ವ್ಯವಸ್ಥಾಪನಾ ಮಹಾವಿದ್ಯಾಲಯ BMS Institute of Technology and Management

(An Autonomous Institution Affiliated to VTU, Belagavi)  
Avalahalli, Doddaballapur Main Road, Bengaluru – 560119

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### Installation & Training on Synopsys EDA tool (C2S) for Digital IC Design

In association with VLSI Minds

### Report

|                                                                                 |                                                                                                    |
|---------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|
| <b>Date:</b><br>24-26 November 2025                                             | <b>Participants:</b><br>M.Tech. VLSI System Design students, Faculty & Staff, Dept.of ECE, BMSIT&M |
| <b>Resource Person:</b><br>Mr. Chetan Kumar N S, CTO & Lead Trainer, VLSI Minds |                                                                                                    |

The Department of ECE, BMSIT&M, obtained the EDA tools from MeITY-CDAC through C2S program. BMSIT&M, is one of the 390 institutions who have obtained this facility in India. In this regard a training program was scheduled on Synopsys EDA tool utilization for Digital IC design. The program is successfully completed. The detailed report as below.

### Day 1: CMOS Design Fundamentals & Schematic Simulation

#### Session Overview:

The first day of the workshop introduced participants to the foundational concepts of **Digital IC Design** and the **ASIC design flow**, followed by hands-on exposure to **Synopsys Custom Compiler** for schematic design and simulation.

#### Topics Covered:

- Introduction to VLSI & ASIC Design Flow, full-custom IC design methodology
- Synopsys Custom Compiler Environment
- Creating new projects and libraries
- Understanding design hierarchy and file organization
- Setting up technology libraries and PDK integration
- CMOS Circuit Fundamentals, Structure and behavior of PMOS and NMOS
- Schematic Entry, Symbol creation
- CMOS Inverter



## **Day 2: Layout Design, DRC & LVS Verification**

### **Session Overview:**

The second day focused on physical implementation using the Custom Compiler Layout Editor. Participants translated their schematics into mask-level layouts and learned to validate physical correctness.

### **Topics Covered:**

#### **Layout Design Concepts:**

Understanding layers and mask generation, Diffusion, poly, metal, and contact design basics, Importance of design rule constraints.

Custom Compiler Layout Implementation for CMOS Inverter

#### **Design Rule Check (DRC) Using IC Validator**

Running technology-specific rule checks, Fixing common errors, Minimum spacing violations, Width, enclosure, and overlap issues

#### **Layout vs Schematic (LVS) Verification**

Netlist extraction, Comparing layout netlist with schematic netlist, Removing mismatches (shorts, opens, incorrect pin connections)

### **Day 2 Outcome:**

Participants completed layouts for multiple CMOS circuits, executed full DRC and LVS verification, and resolved errors to achieve sign-off-compliant layouts.



### **Day 3: RC Extraction, Post-Layout Simulation & Advanced Design**

#### **Session Overview:**

The final day integrated all design stages into a complete workflow, from layout extraction to post-layout simulation. The session concluded with advanced sequential circuit design and a hands-on mini-project.

#### **Topics Covered:**

**RC Extraction Using StarRC**, Extracting parasitic resistances and capacitances from layouts, **Post-Layout Simulation (HSPICE)**, Back-annotating extracted RC parameters Comparing pre-layout vs post-layout results, Observing delay degradation due to interconnect parasitic.

**The same procedure was carried for NAND gate using 40nm PDK.**

#### **Day 3 Outcome:**

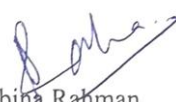
Participants completed the end-to-end flow from schematic to post-layout simulation and gained exposure to sequential digital design. They also developed a mini-project demonstrating applied understanding of all workshop tools.



STTP Coordinators

  
Dr. Banuprakash R  
PG-VSD Coordinator  
Assoc. Professor, ECE

  
Dr. Raju Hajare  
Professor, ECE

  
Dr. Sabina Rahman  
Assoc. Professor, ECE

  
Dr. Jagannath K B  
Assoc. Professor, ECE

  
HoD ECE  
Dr. A Shobha Rani